FIG. 1

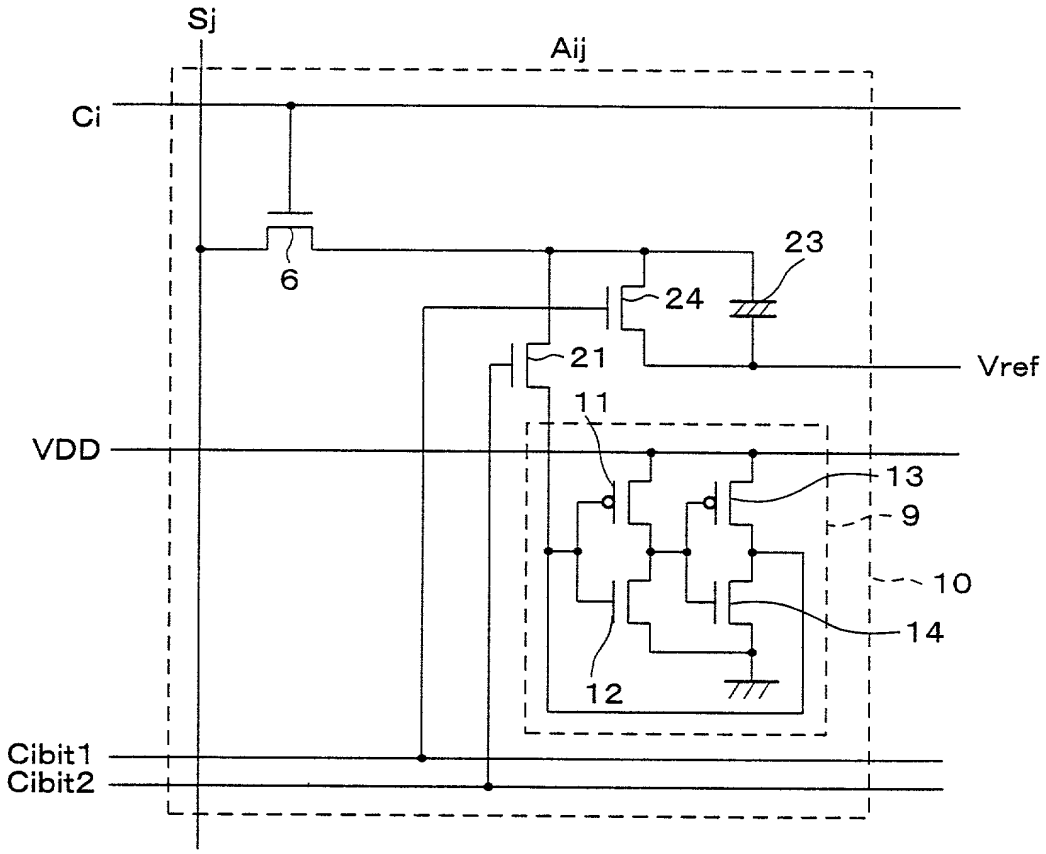


FIG. 2

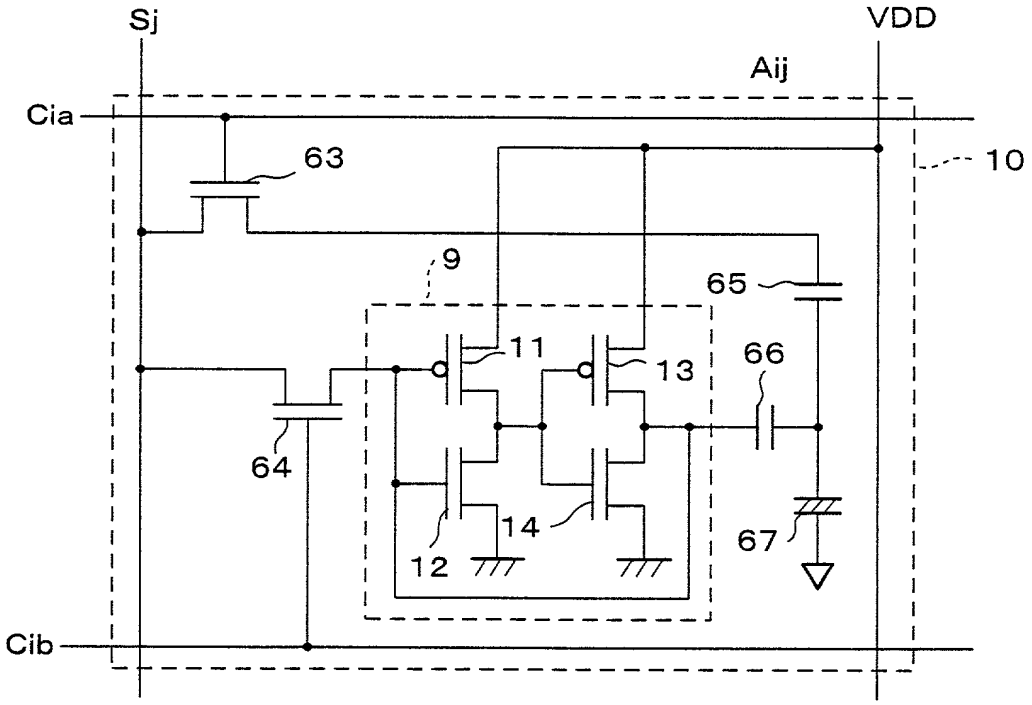
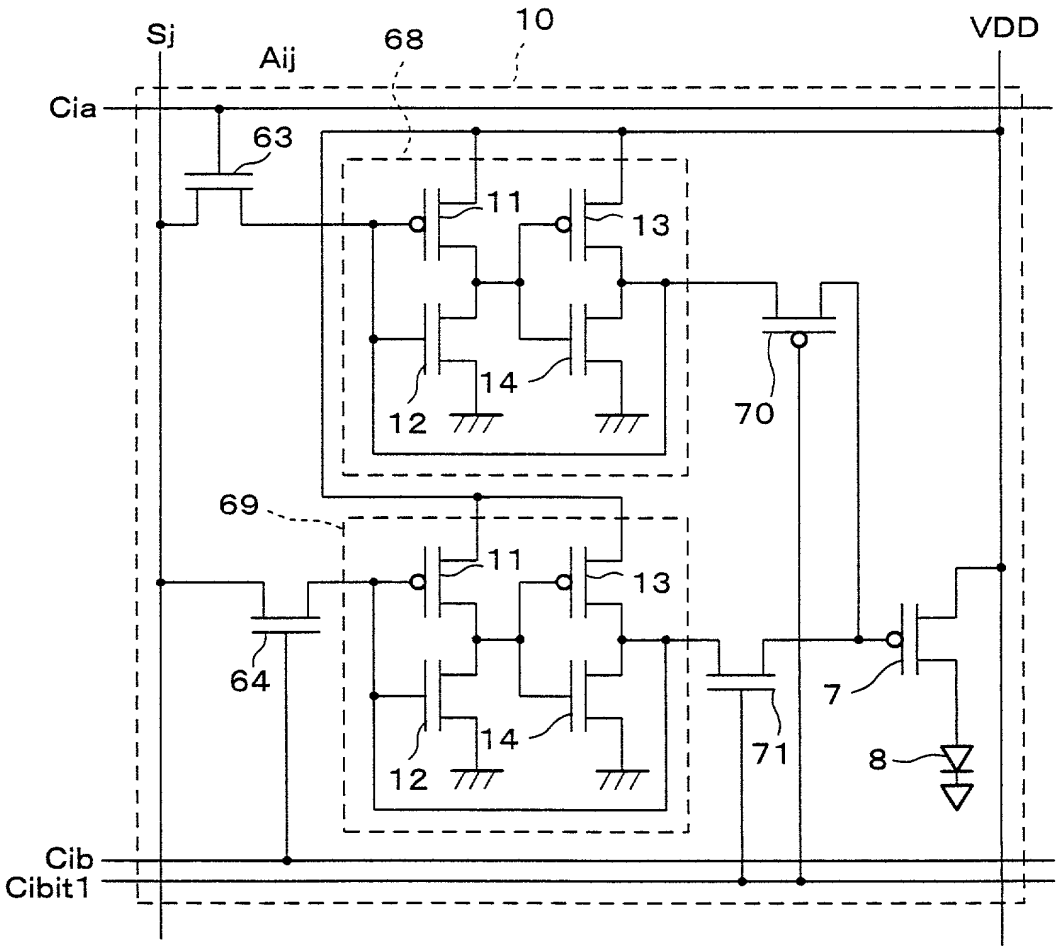


FIG. 3


Sj
Aij
68
10
VDD
Cia
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13
64
14
12
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71
8
Cib
Cibit1

FIG. 4

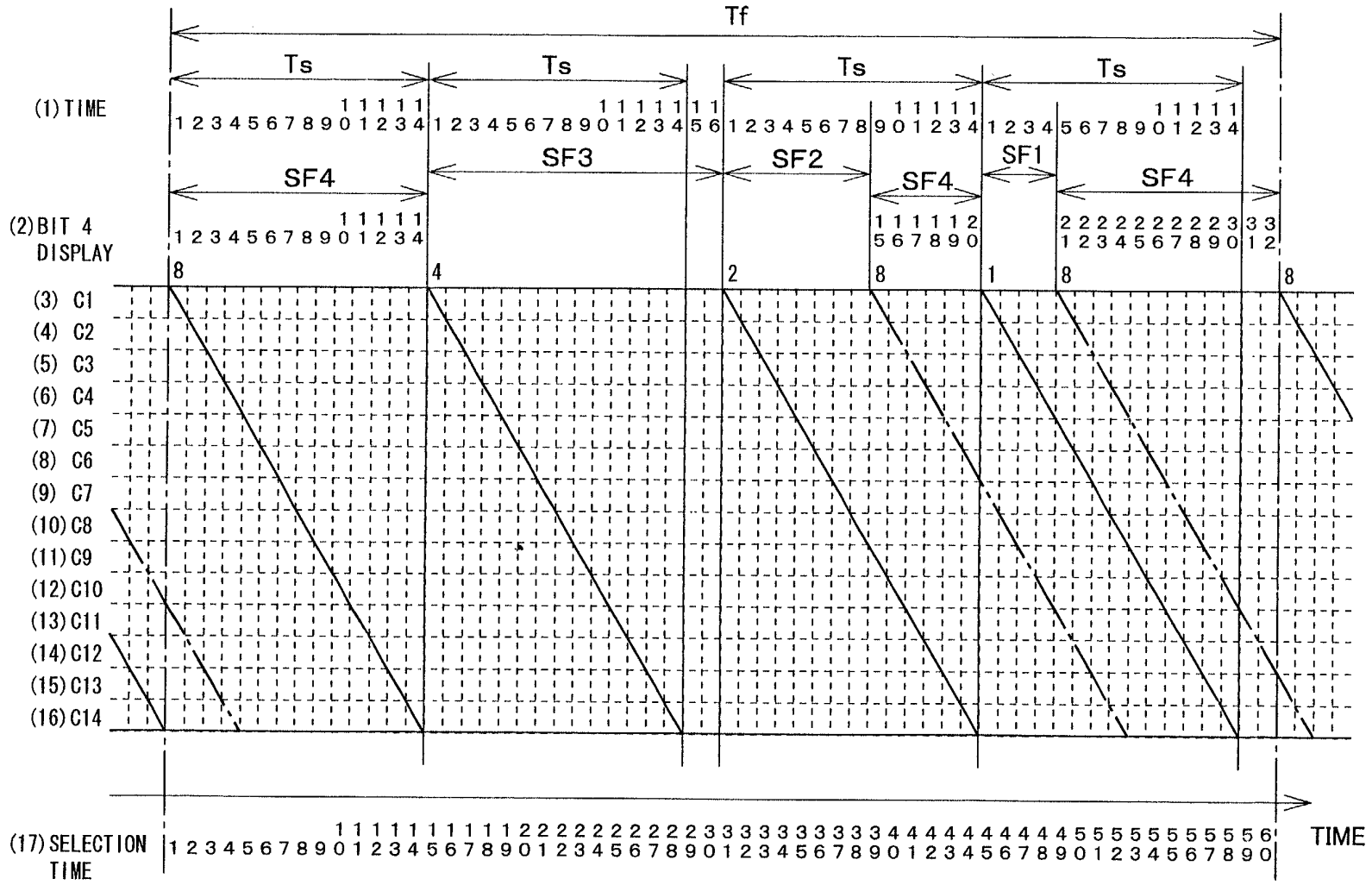

FIG. 5

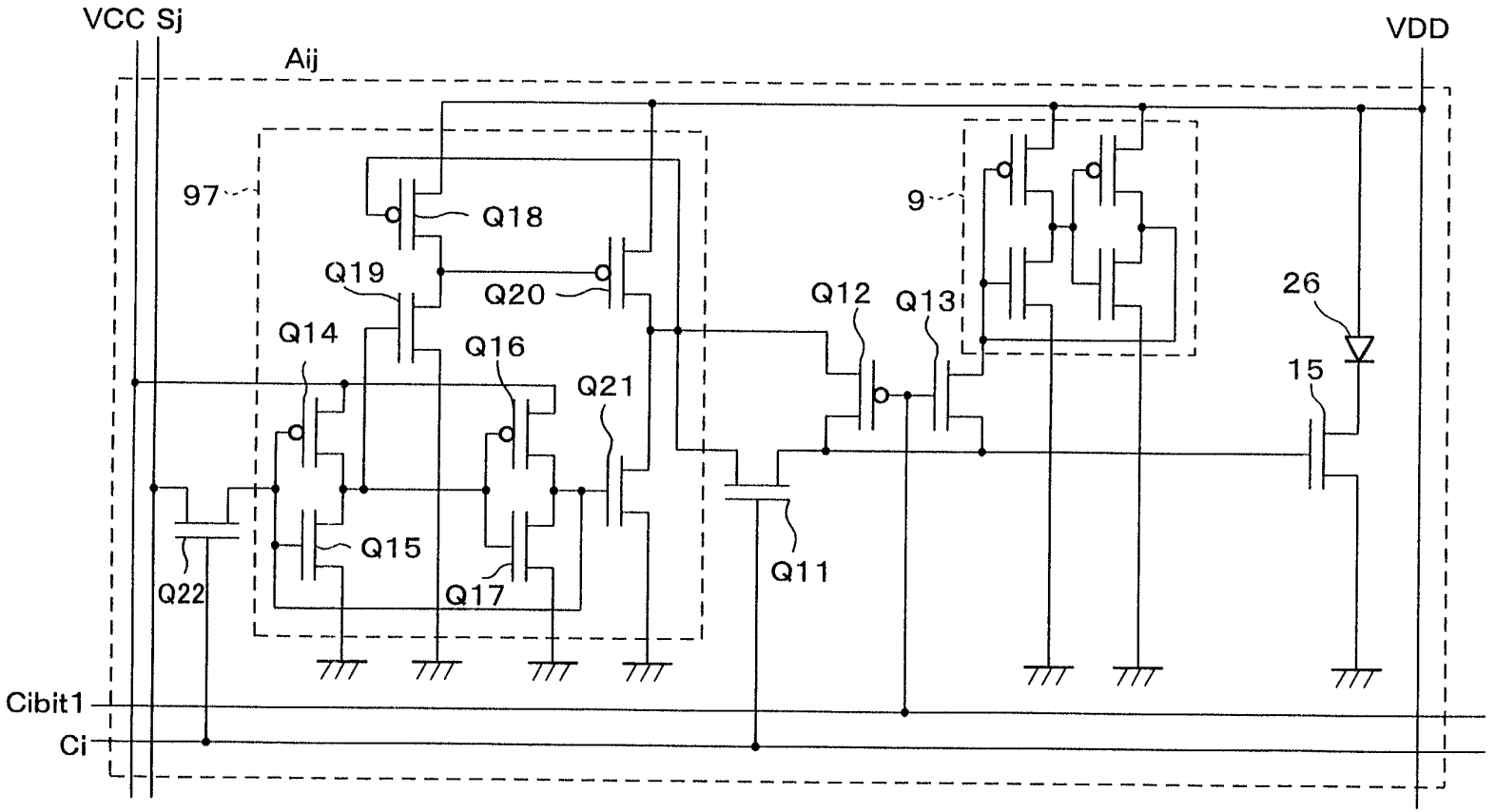

FIG. 6

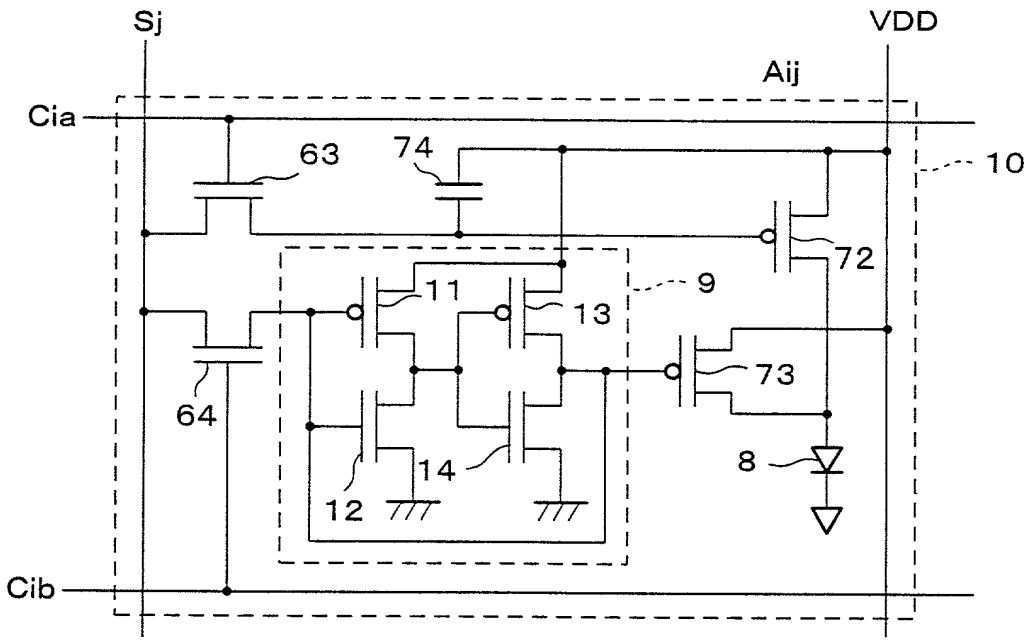

FIG. 7

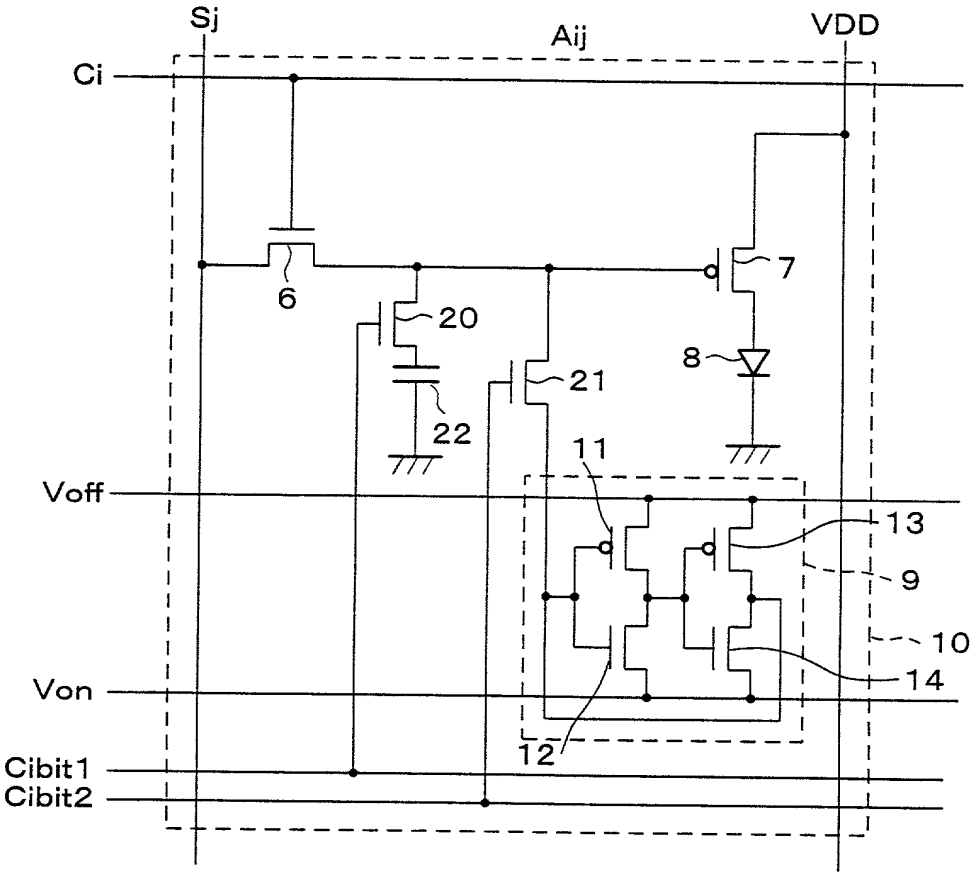

FIG. 8

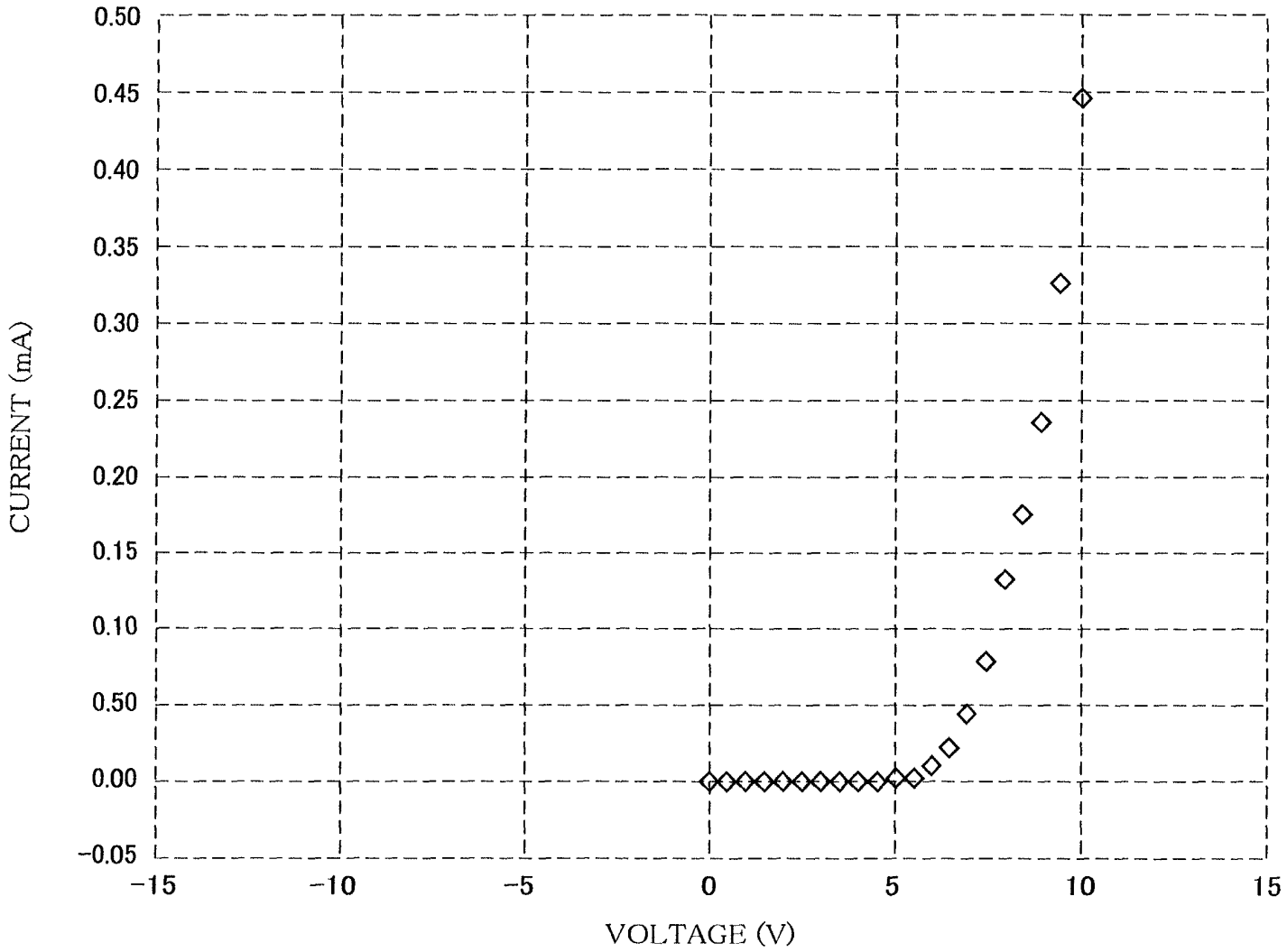

FIG. 9 (a)

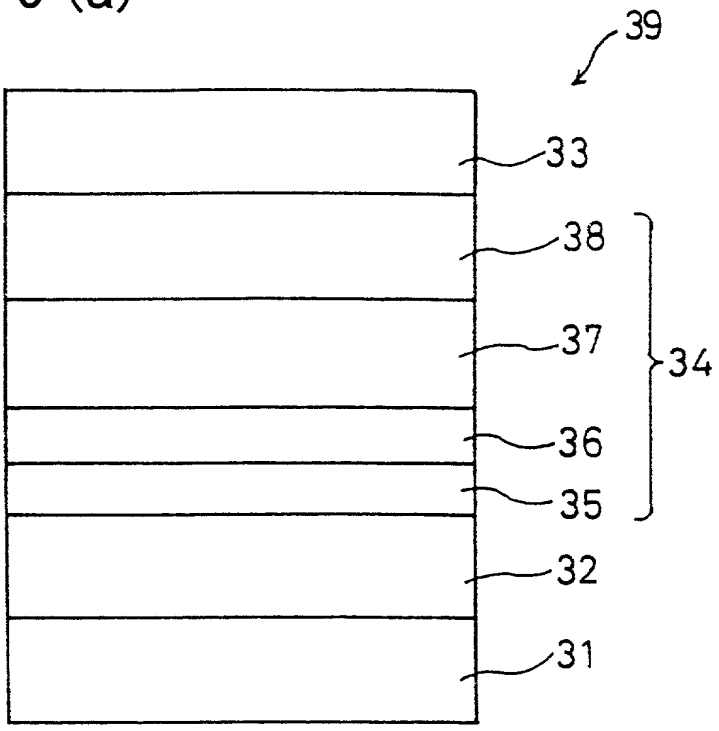

FIG. 9 (b)

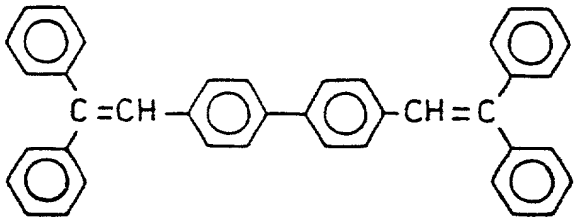

FIG. 10

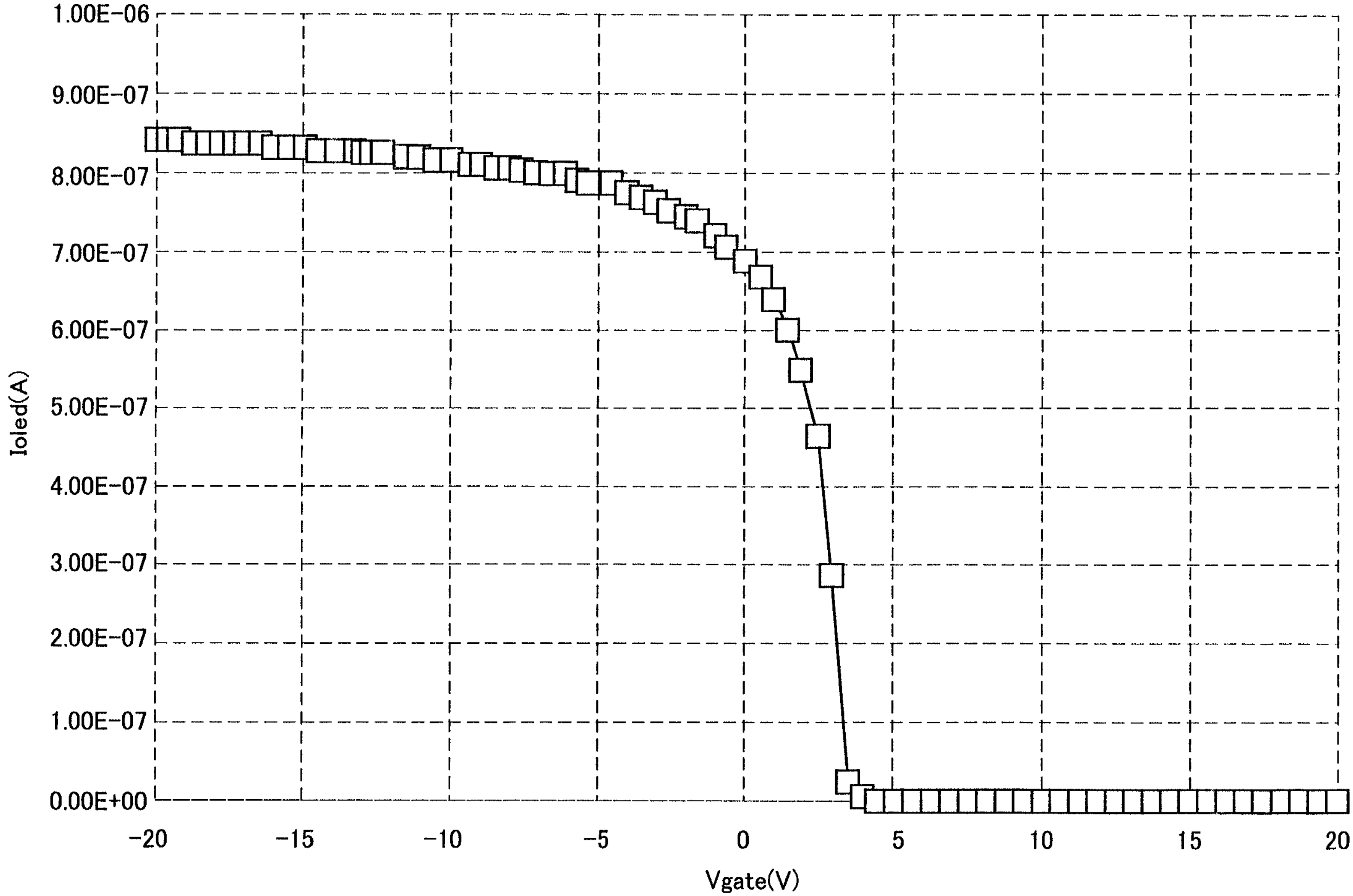

FIG. 11

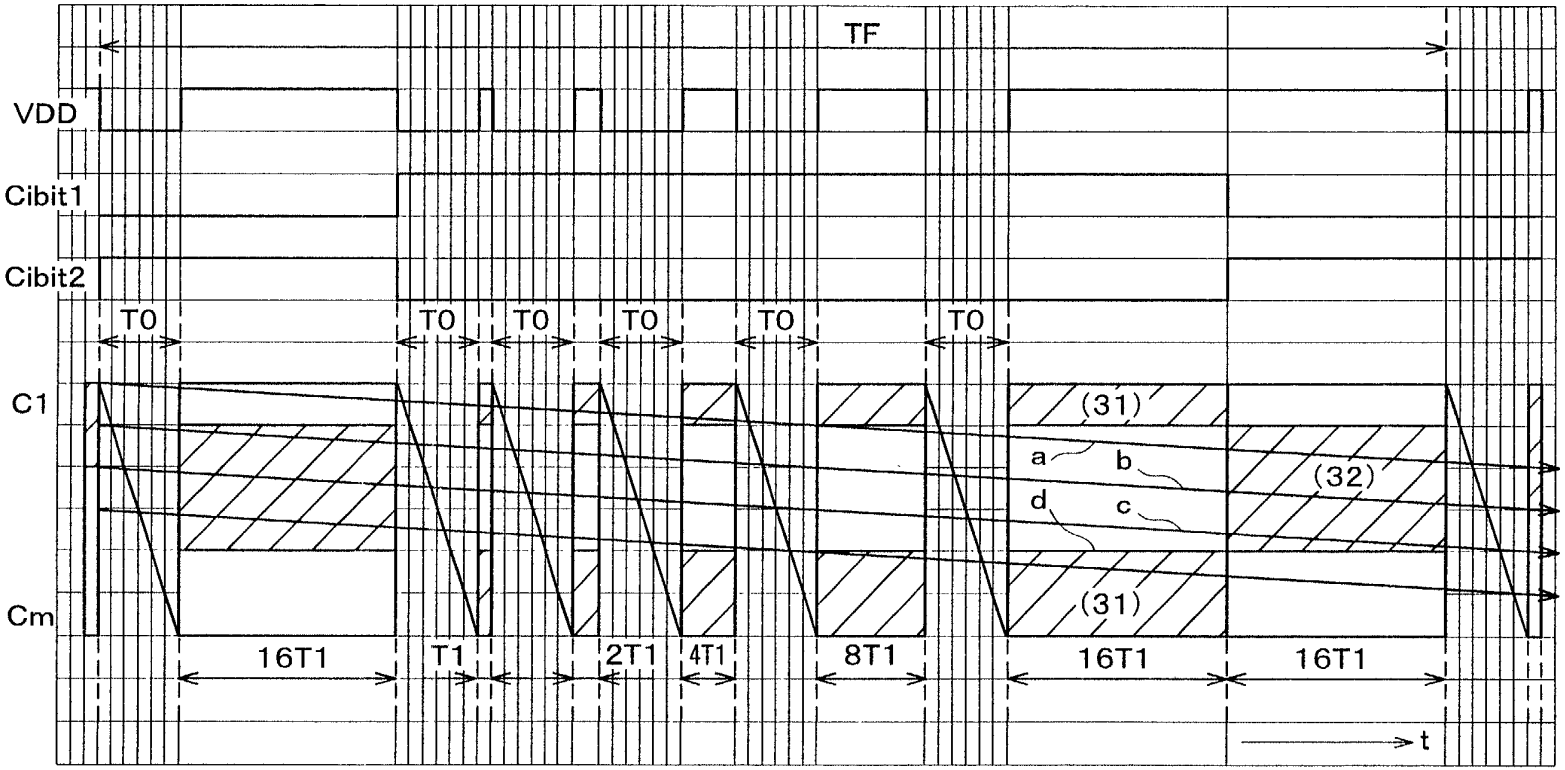

FIG. 12

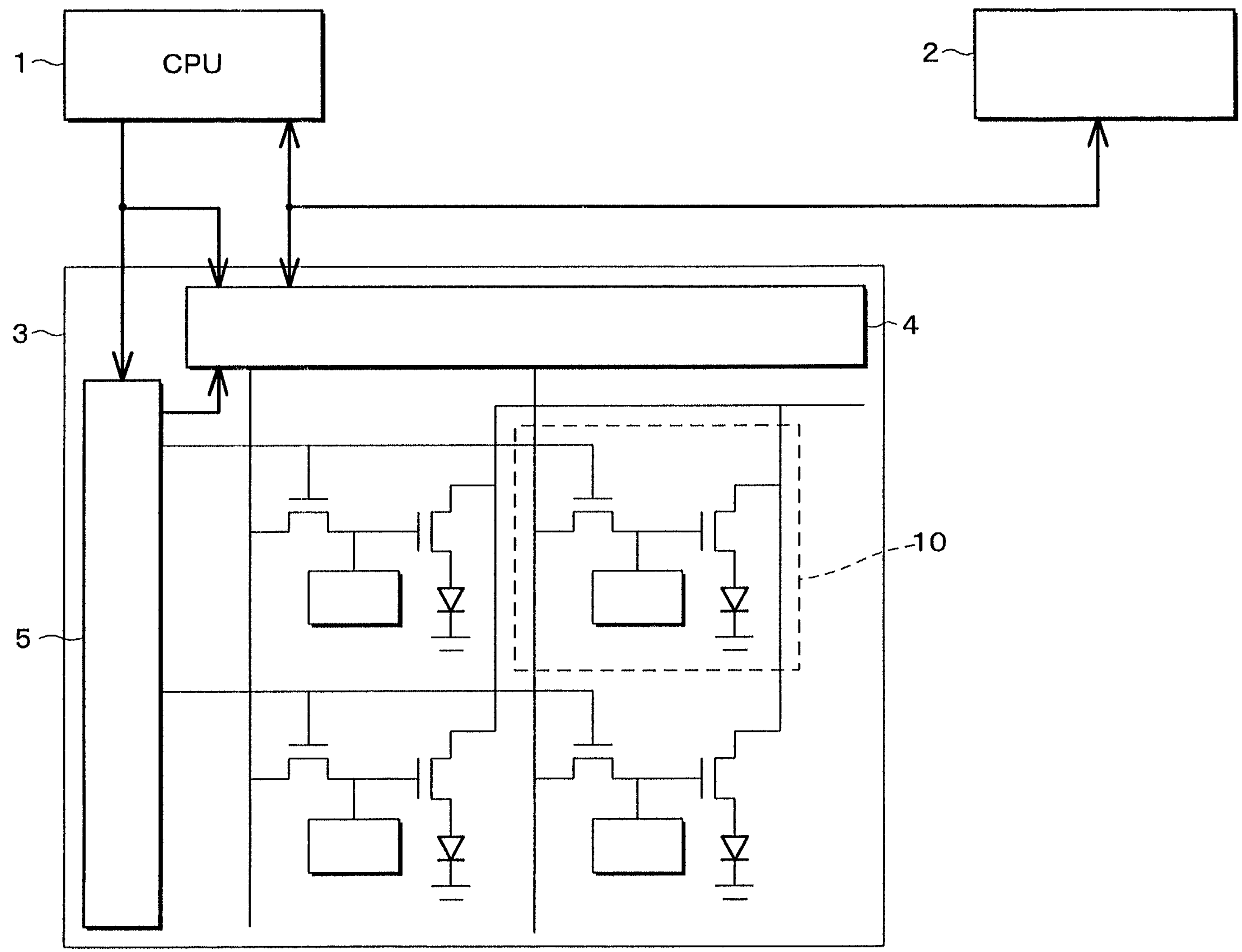

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FIG. 13

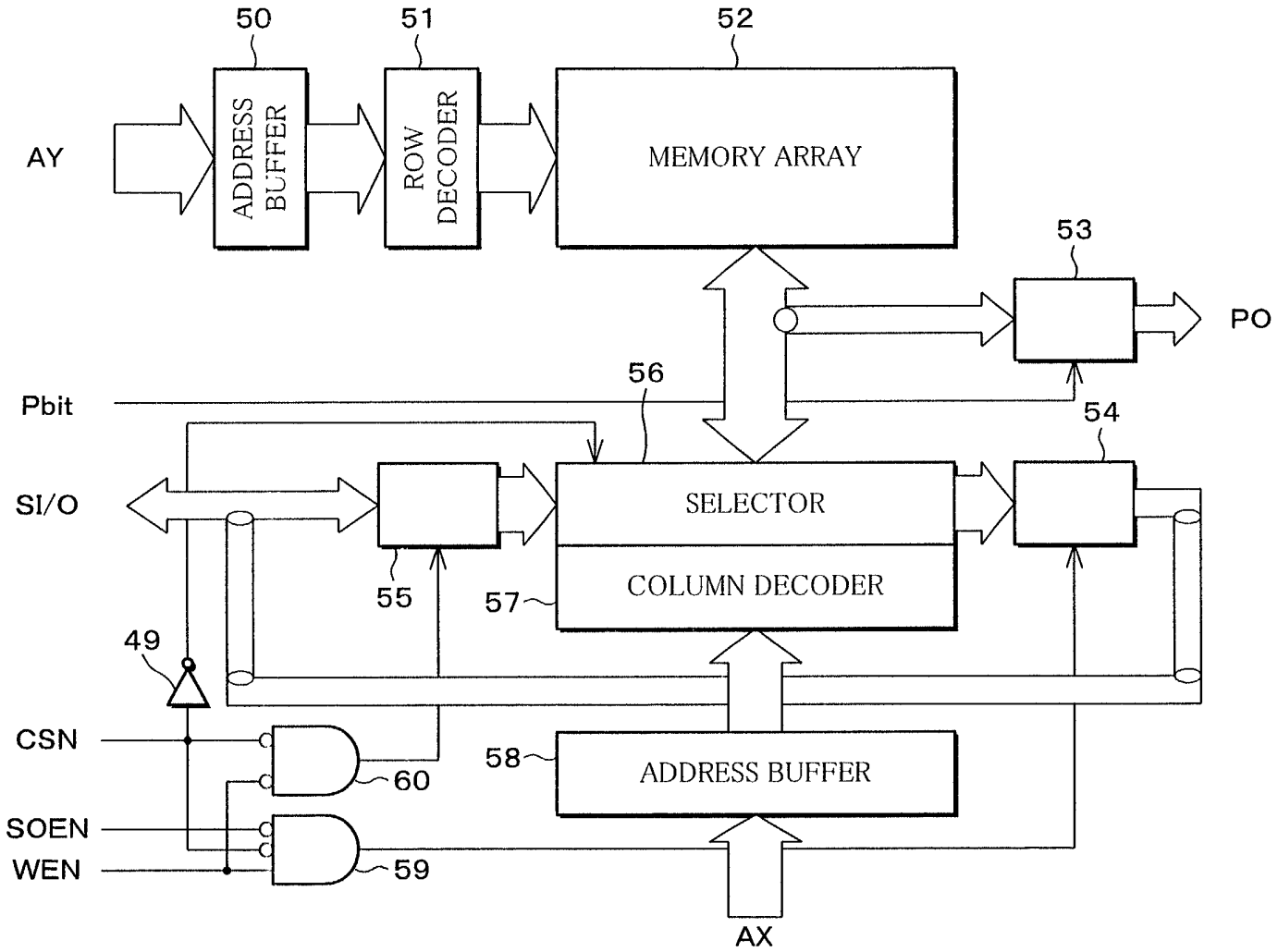


FIG. 14

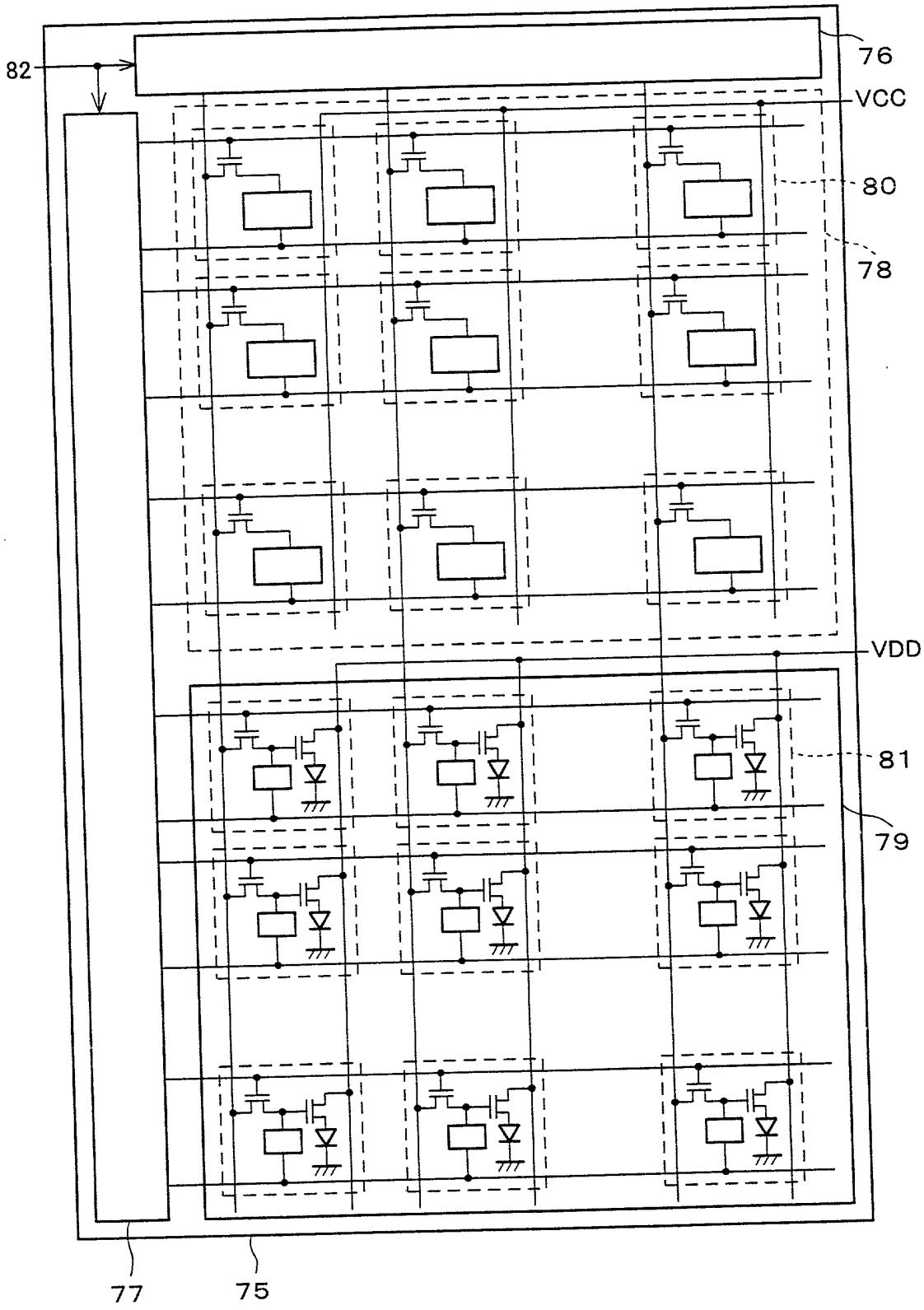


FIG. 15

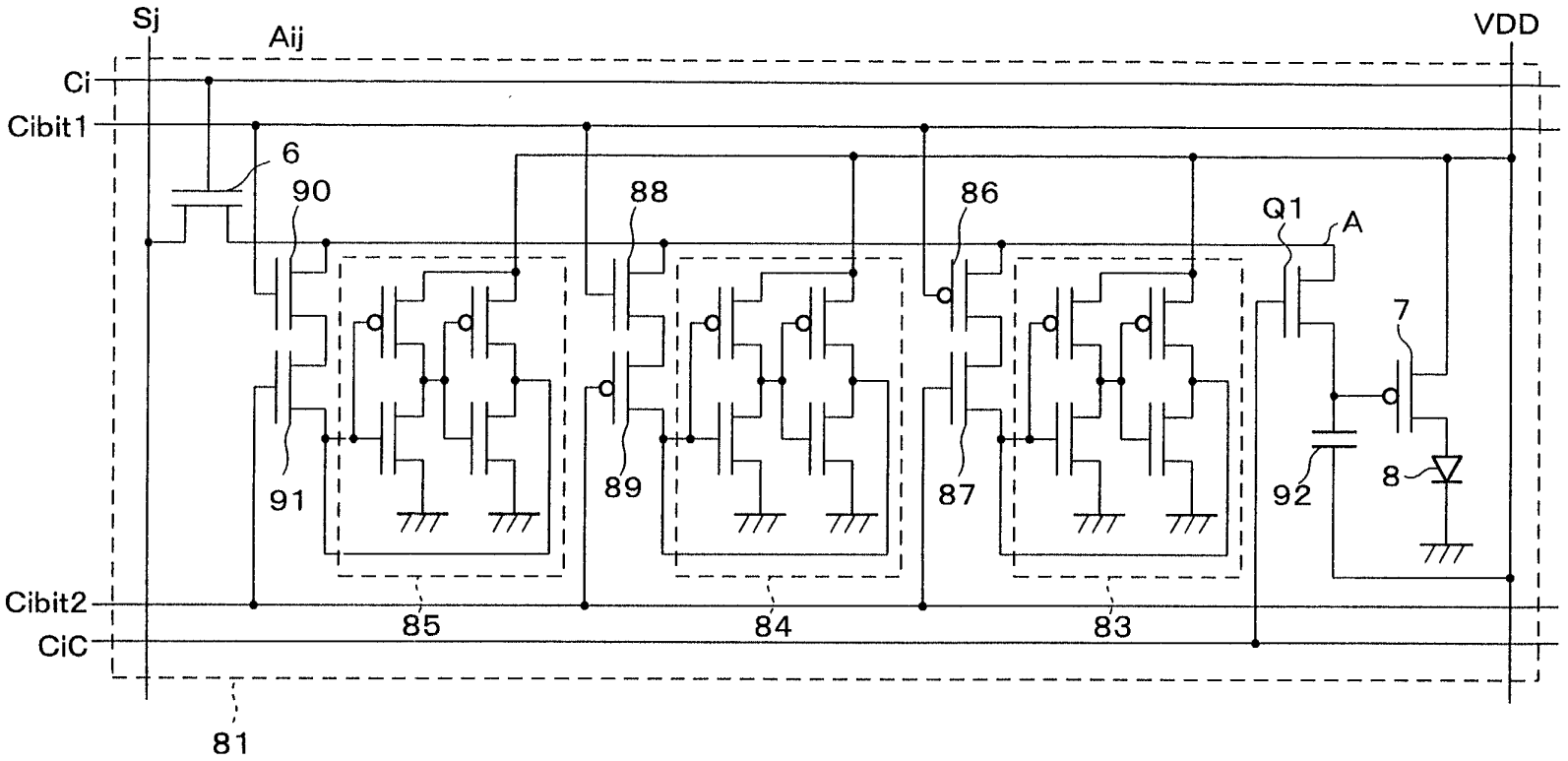


FIG. 16

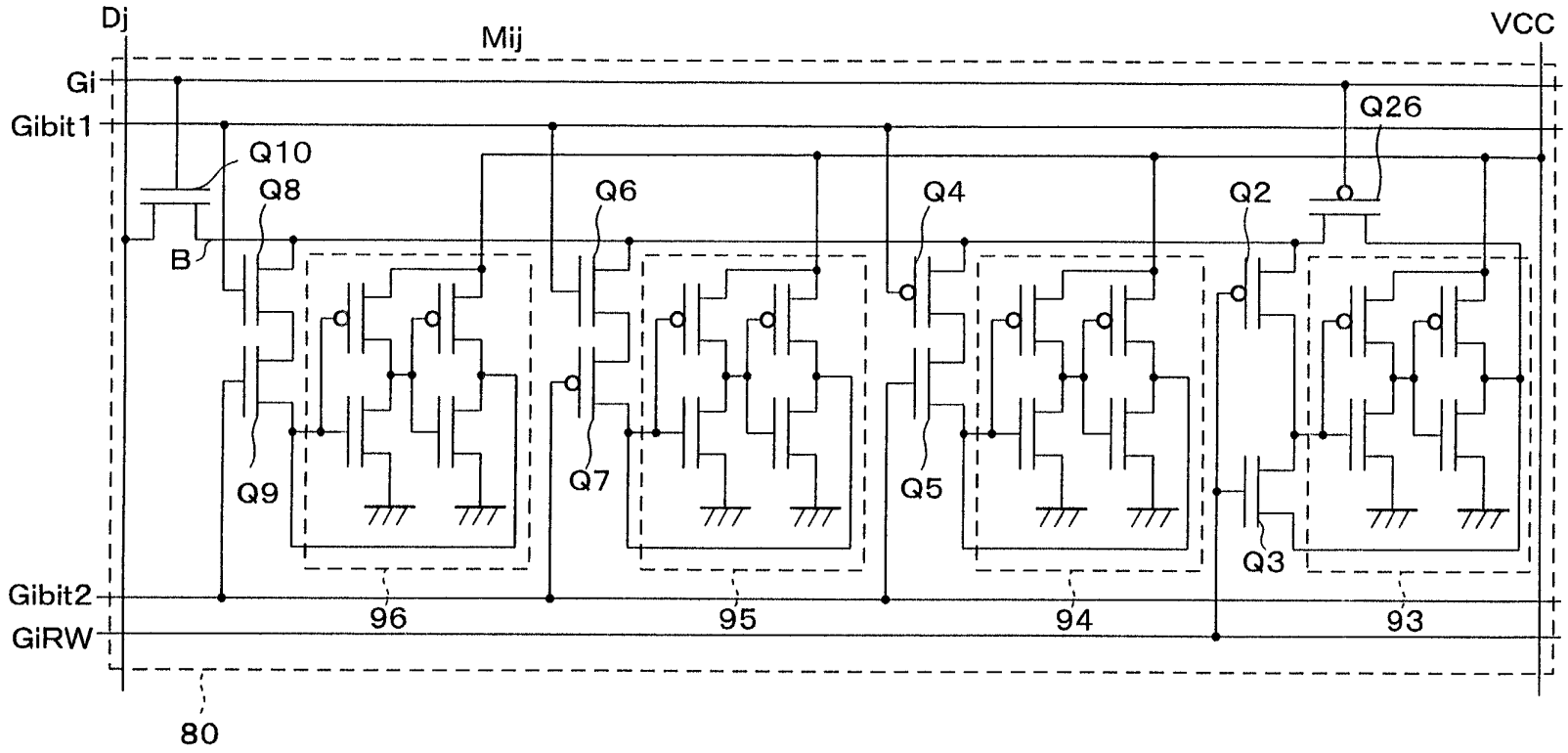


FIG. 17

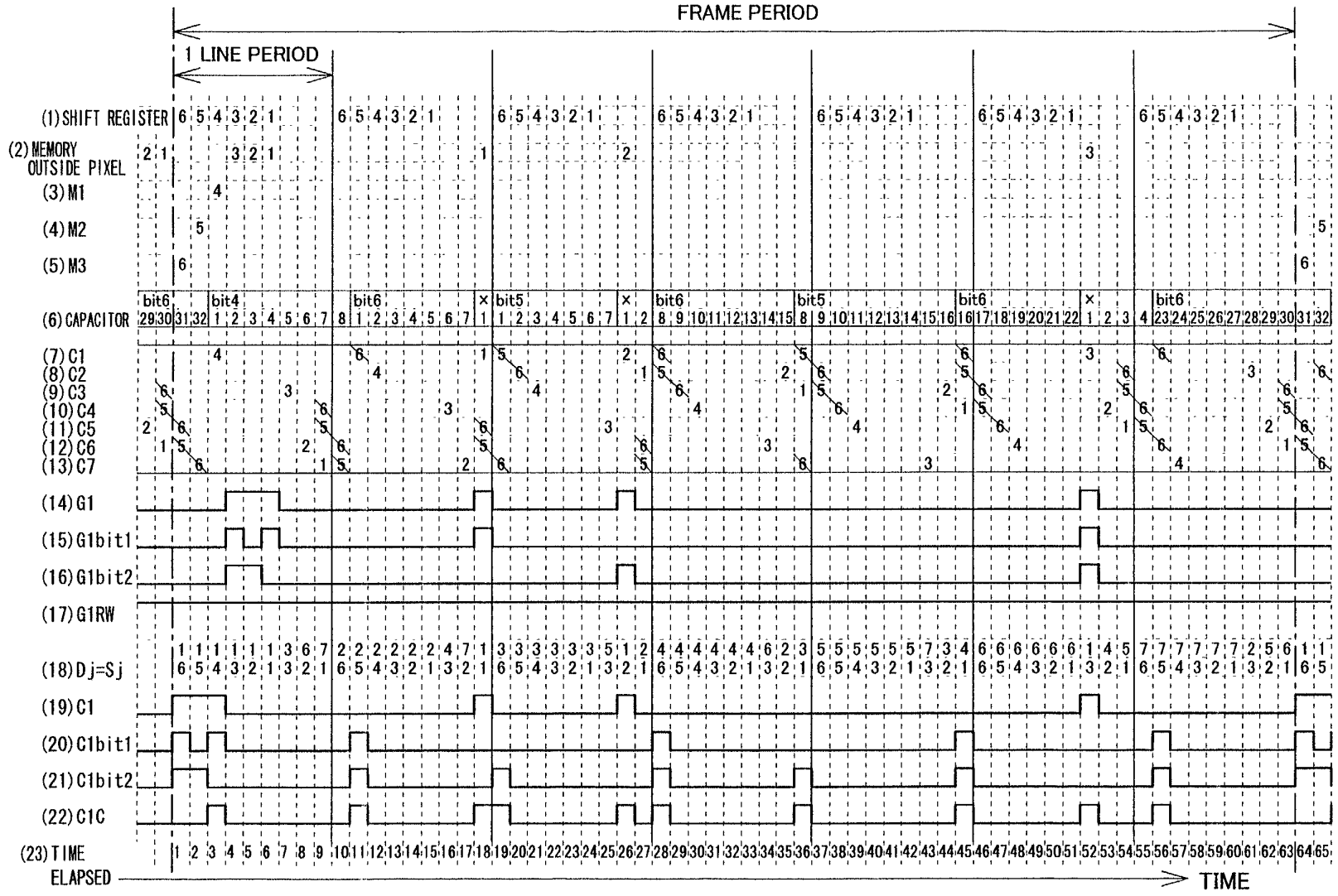


FIG. 18

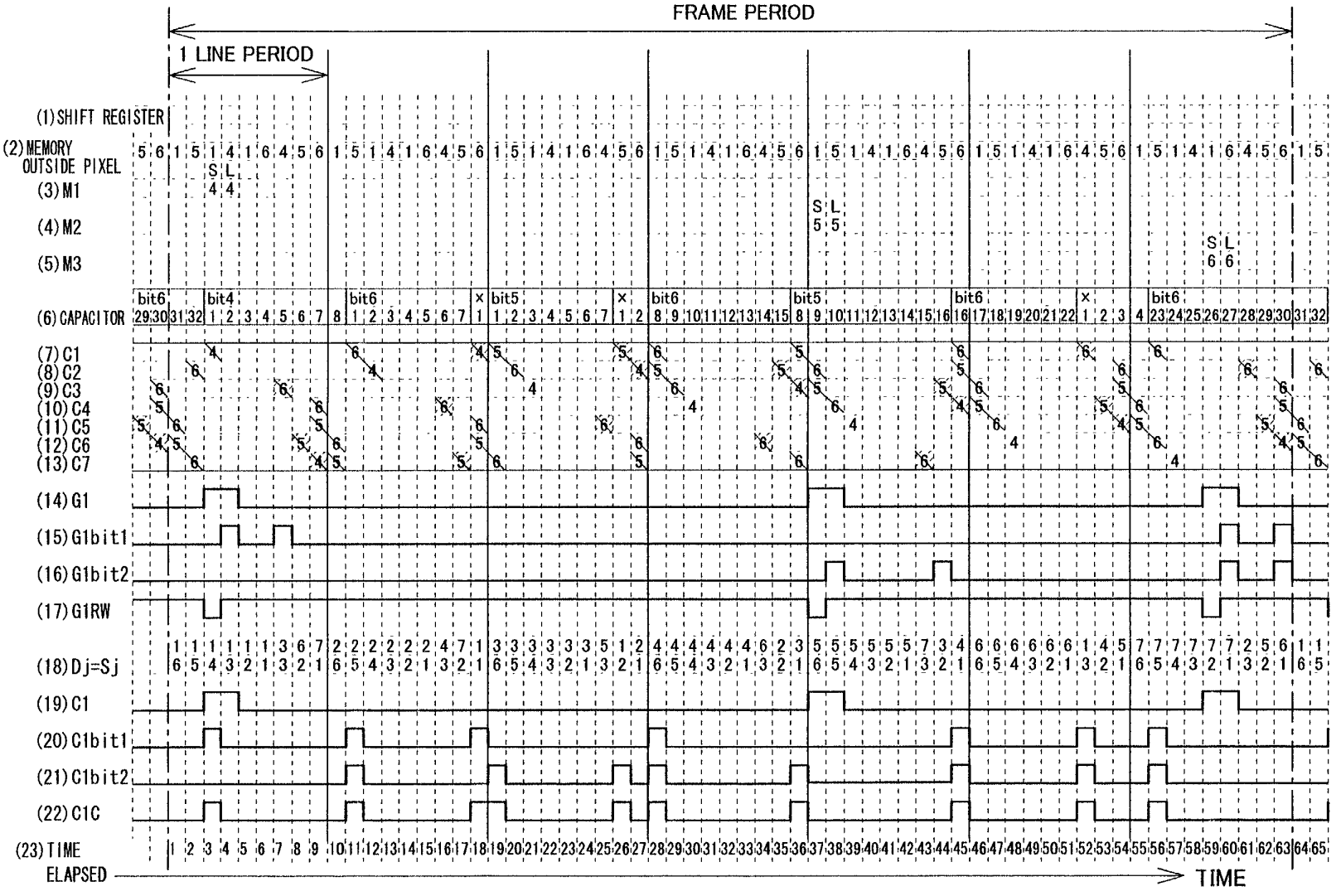
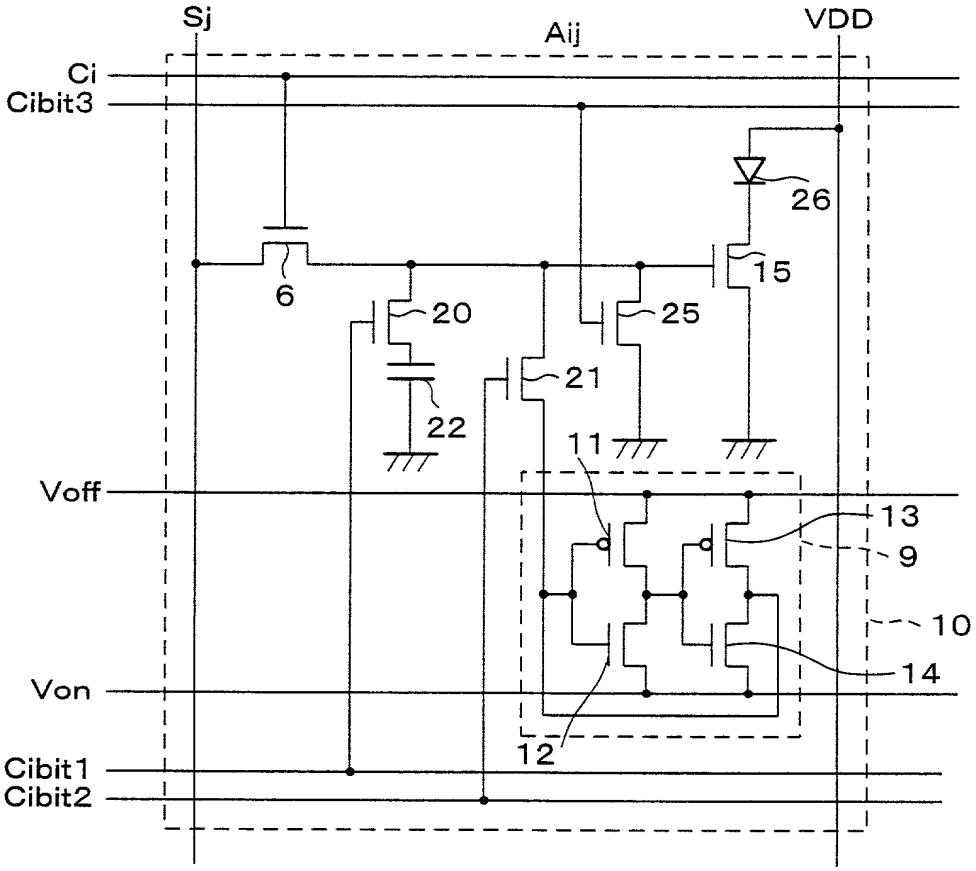


FIG. 19


Sj
Aij
VDD
Ci
Cibit3
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Voff
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Von
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12
Cibit1
Cibit2

FIG. 20

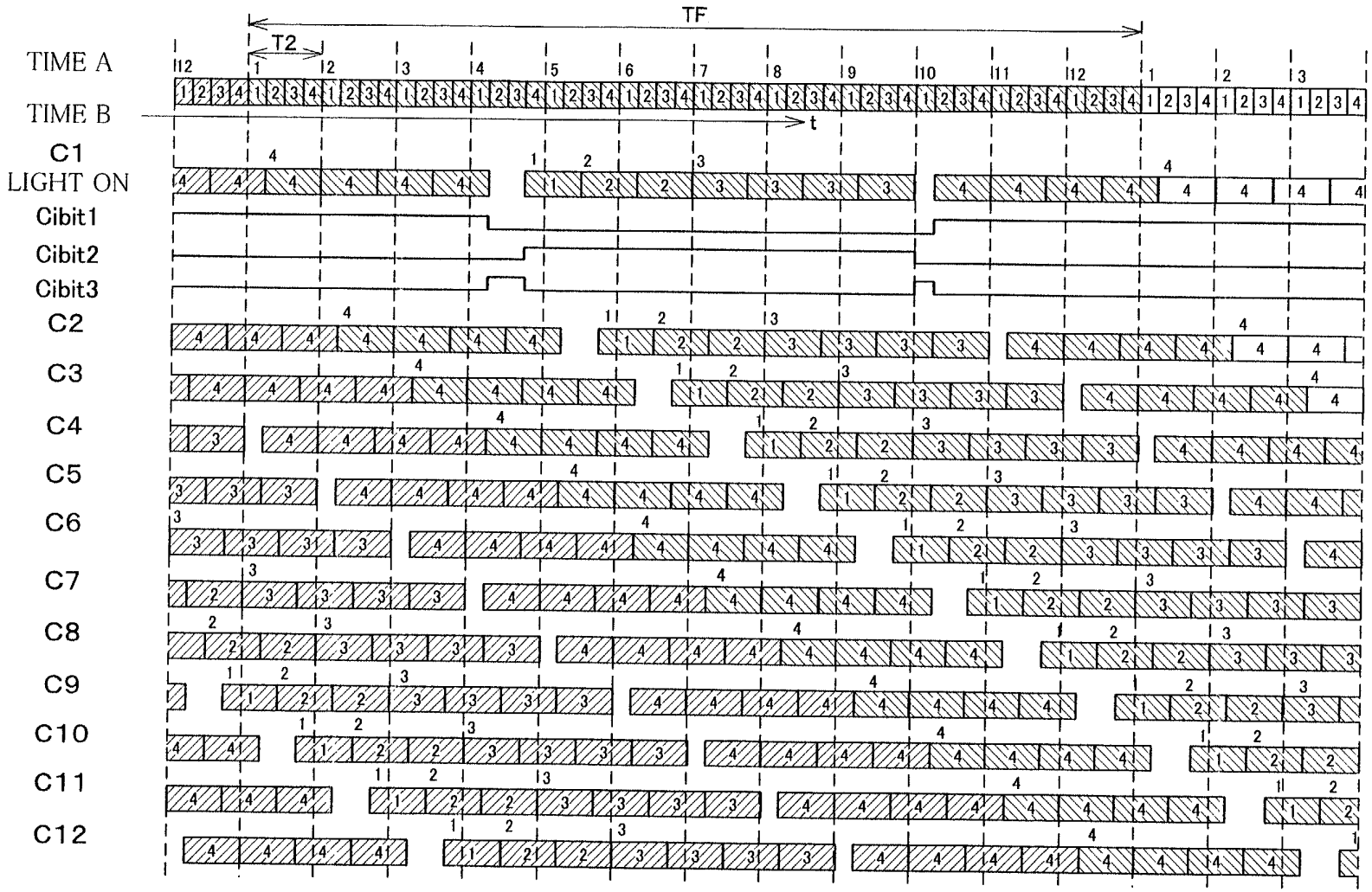

FIG. 21

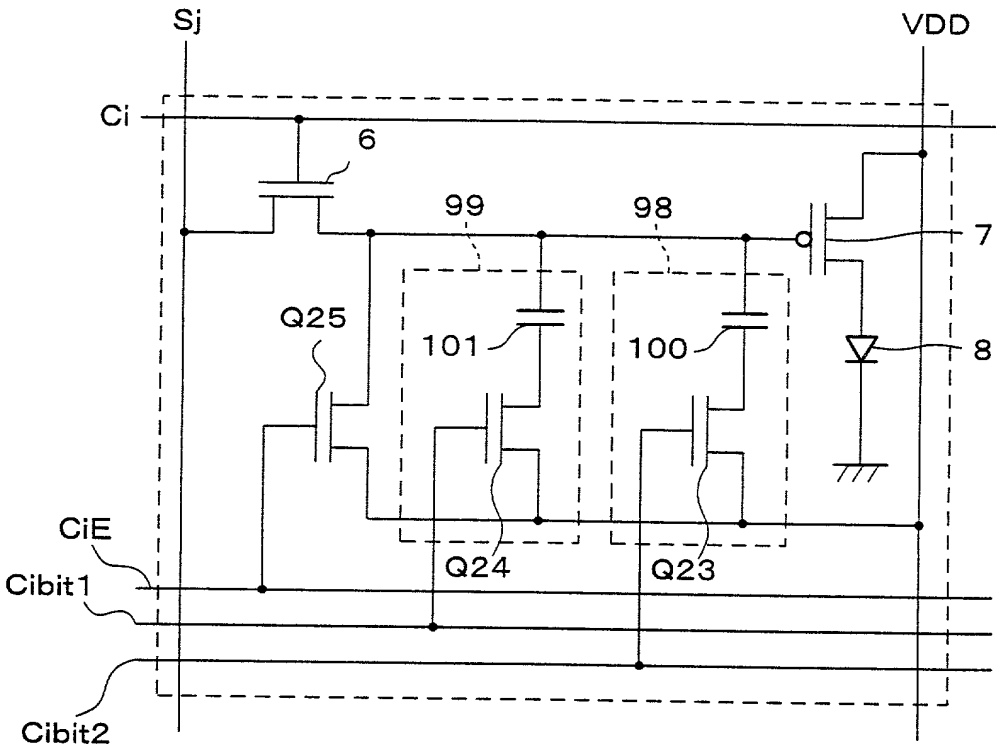

FIG. 22

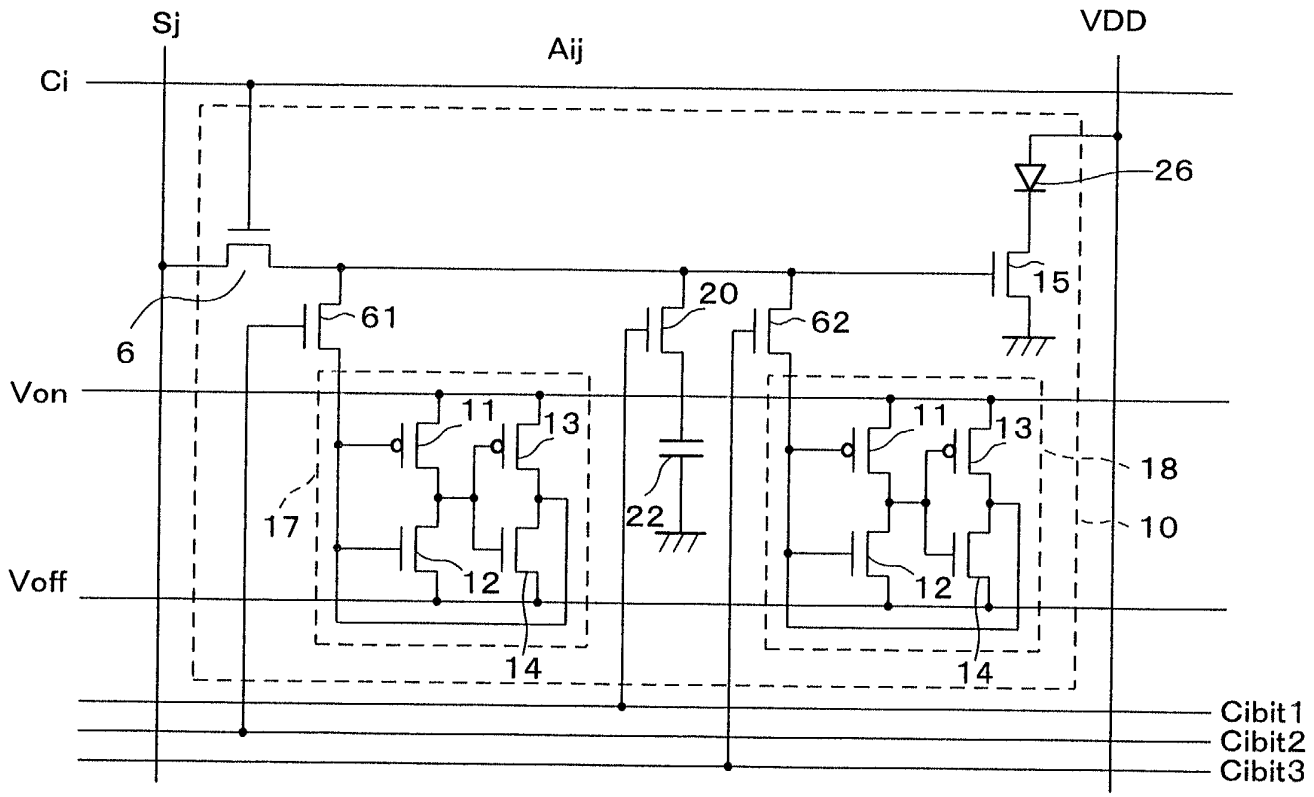

FIG. 23

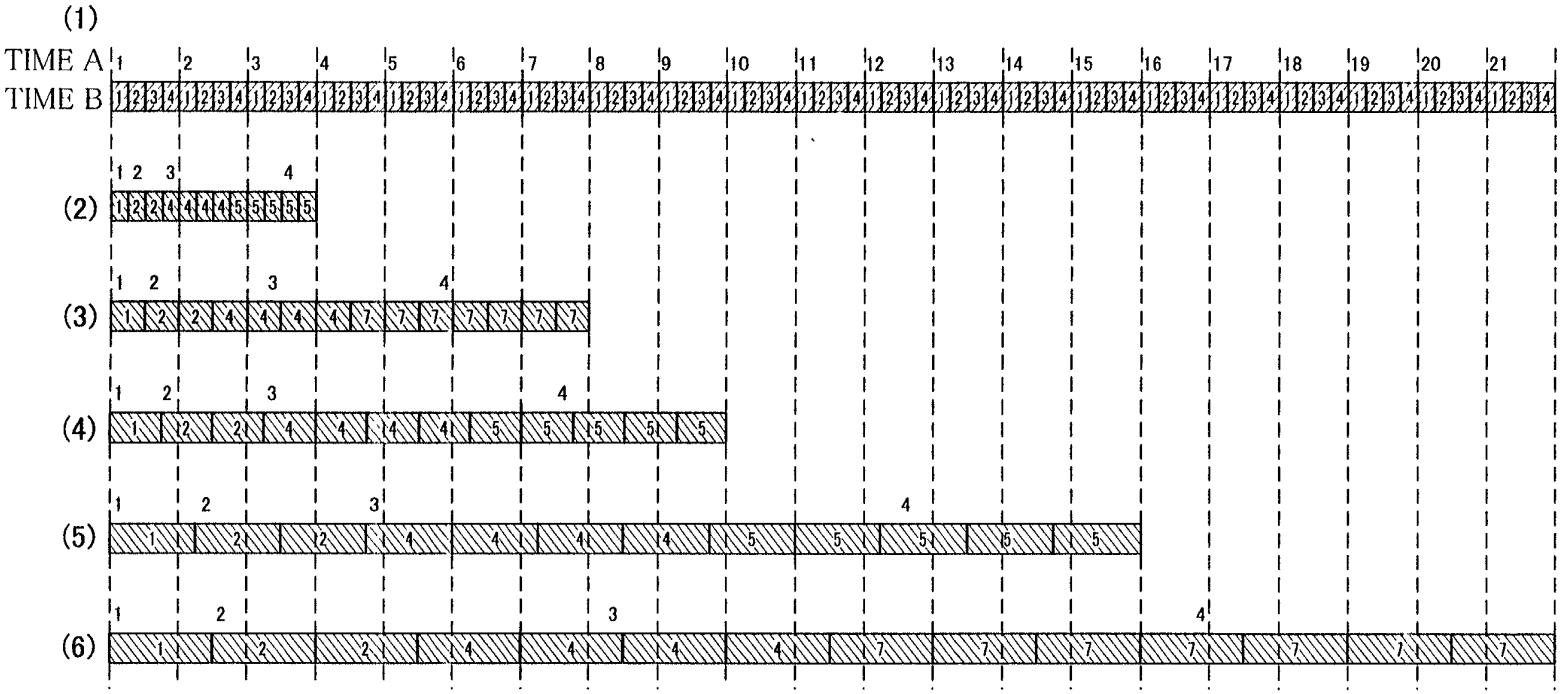

FIG. 24

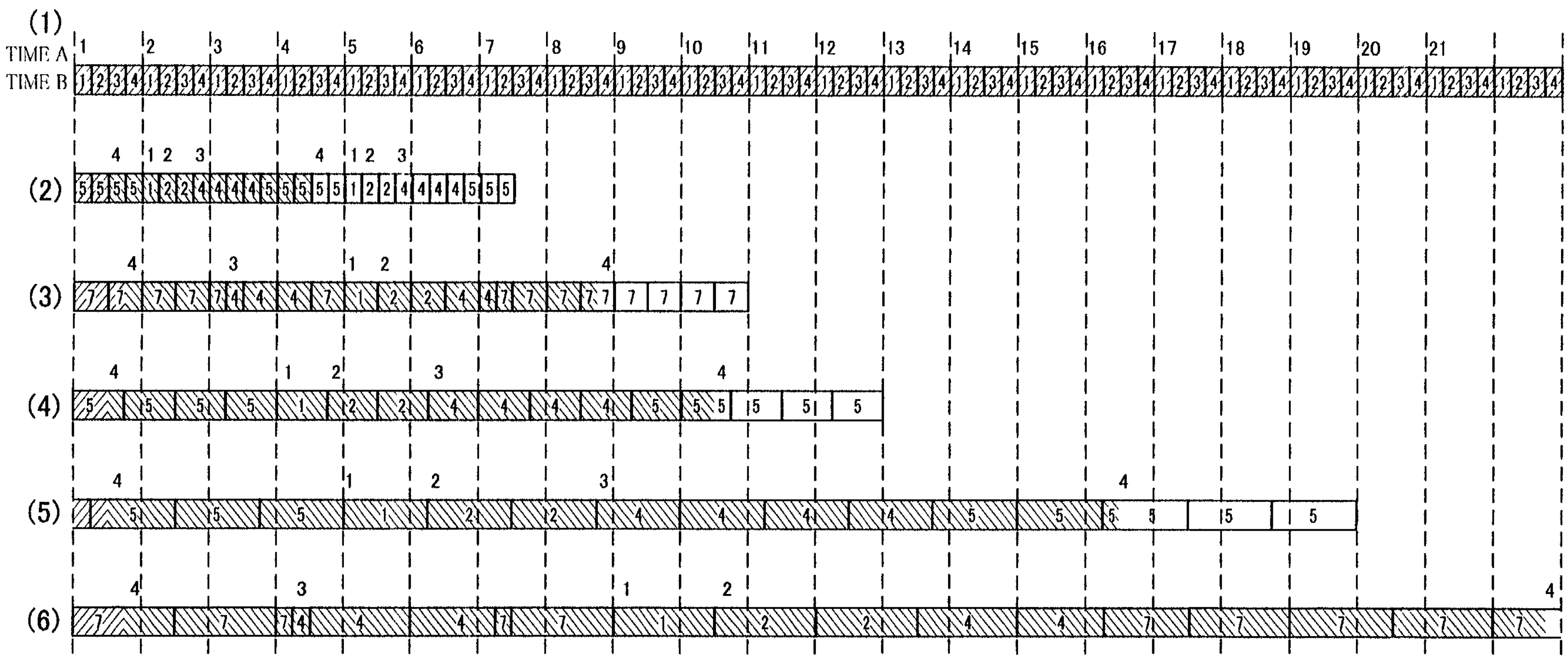

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FIG. 25

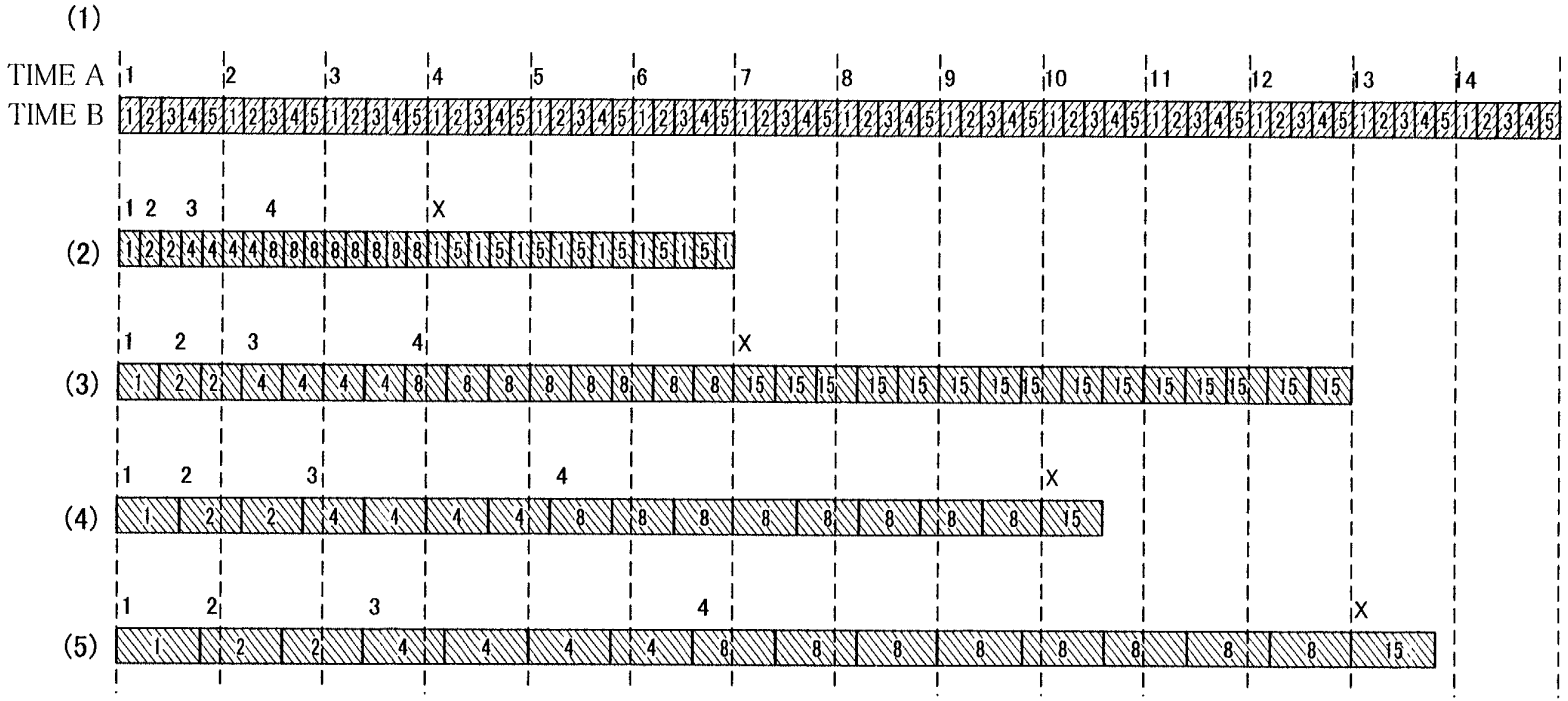


FIG. 26

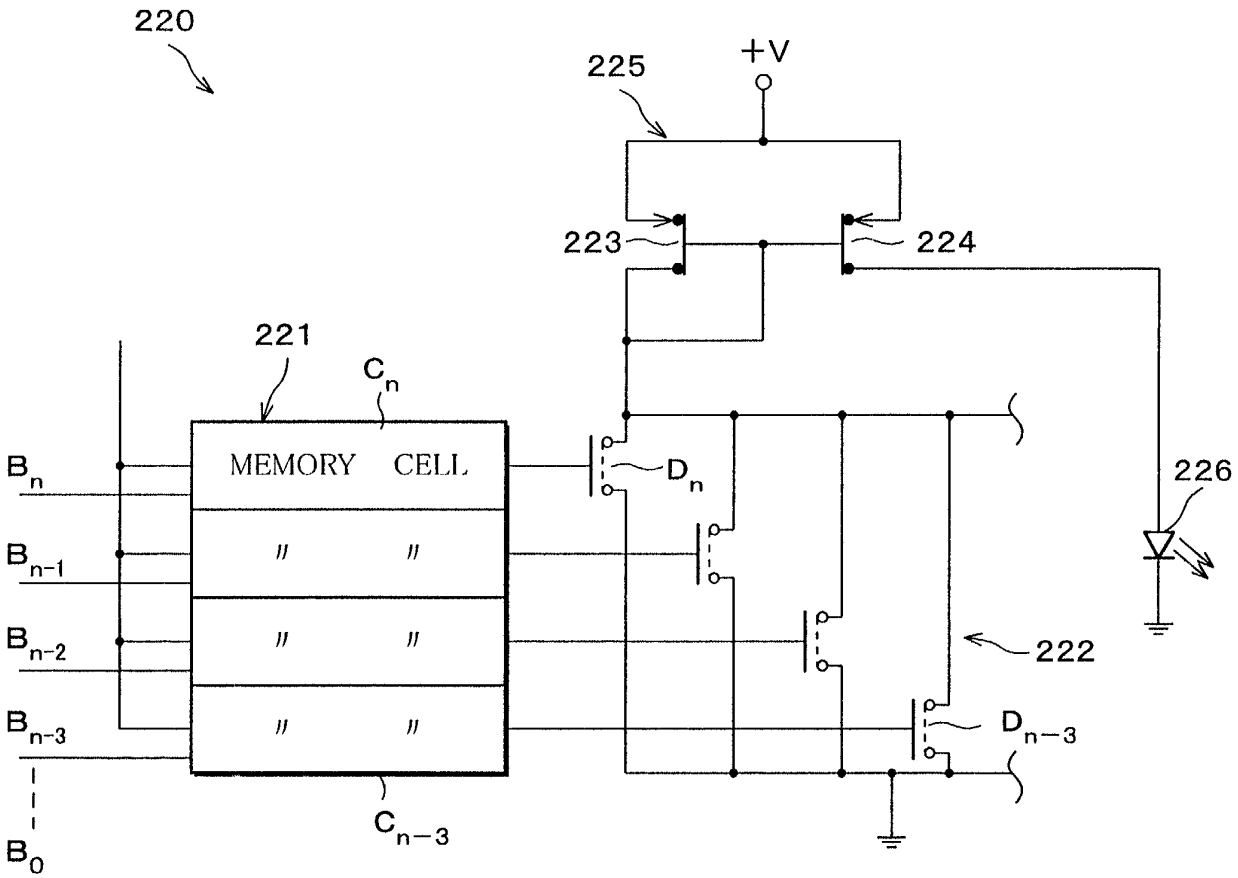


FIG. 27

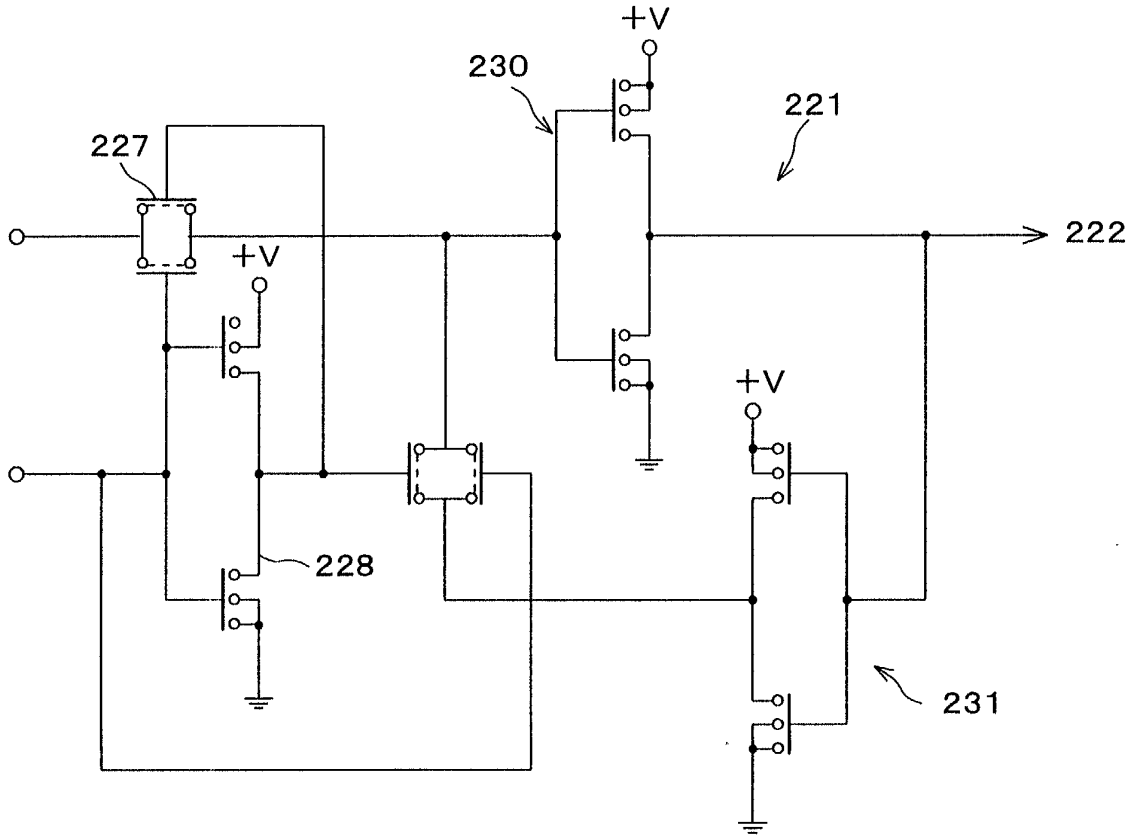


FIG. 28

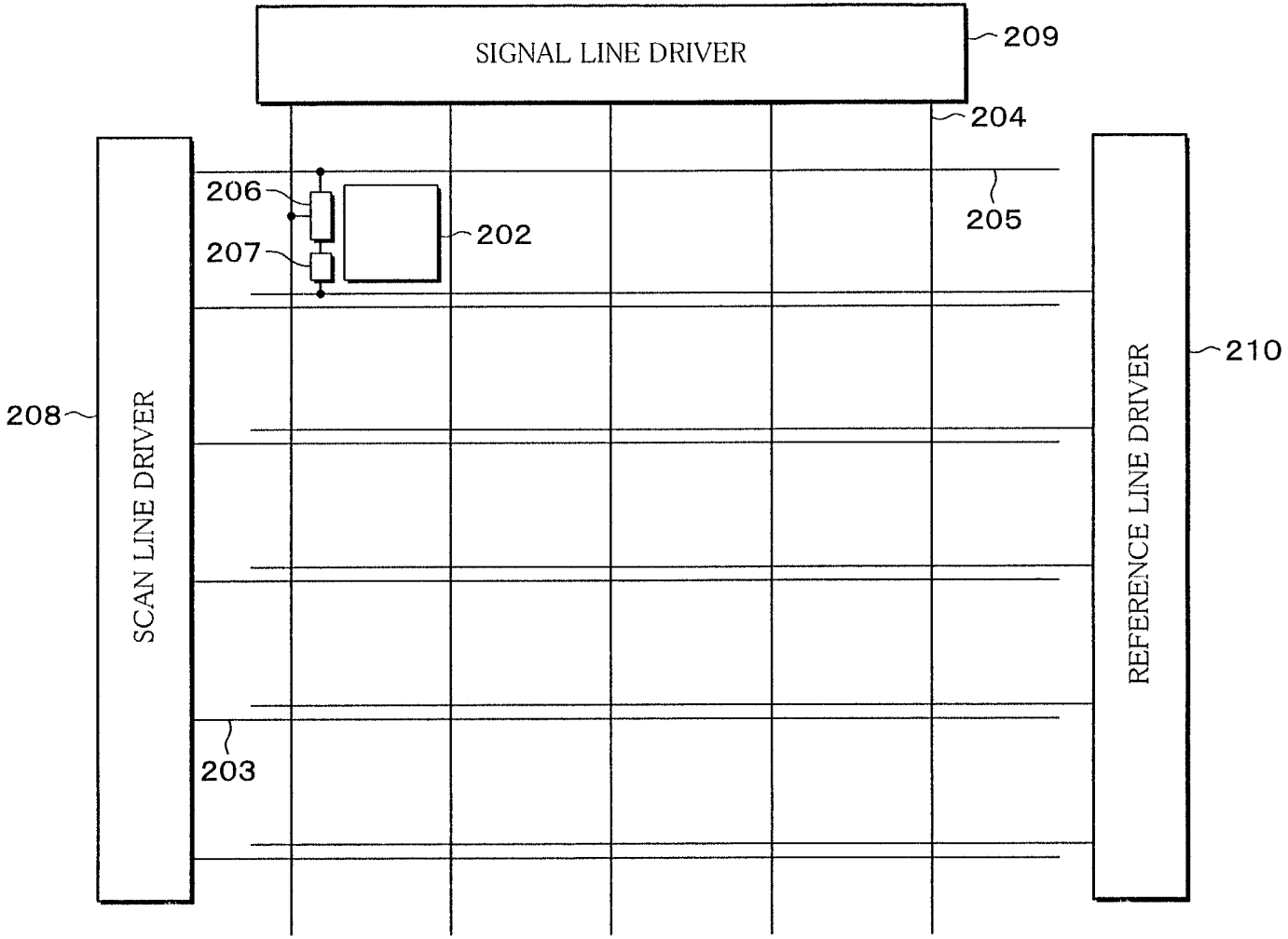
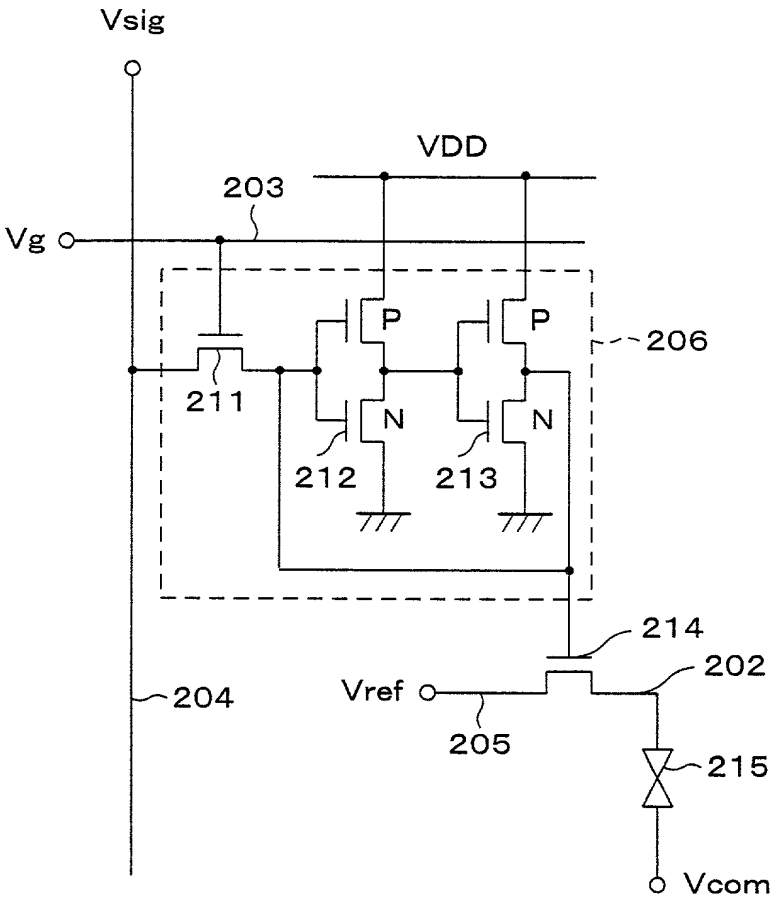


FIG. 29


Vsig
VDD
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Vg
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Vref
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Vcom

FIG. 30

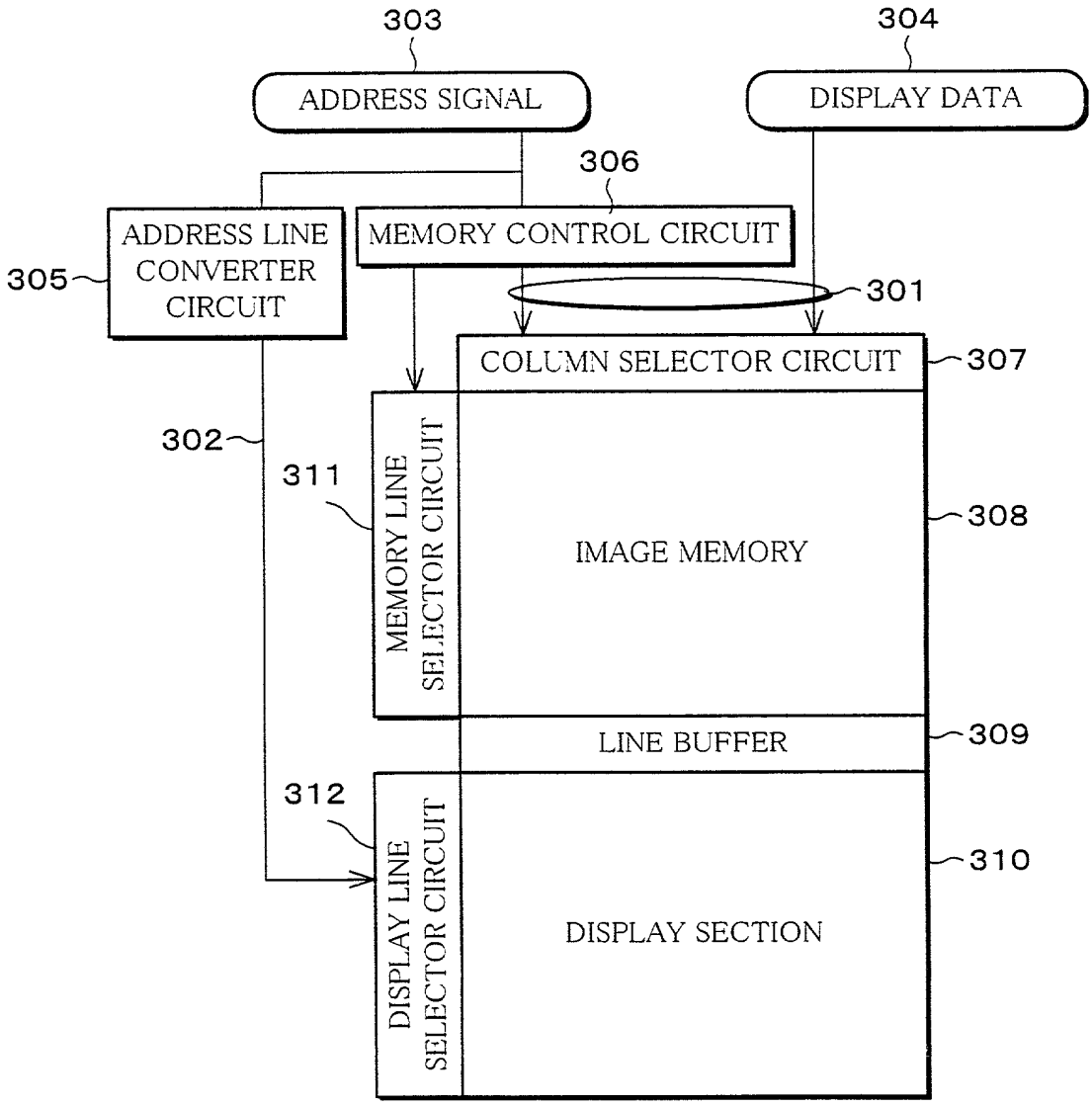
303
304
ADDRESS SIGNAL
DISPLAY DATA
306
ADDRESS LINE CONVERTER CIRCUIT
MEMORY CONTROL CIRCUIT
305
301
COLUMN SELECTOR CIRCUIT
307
302
311
MEMORY LINE SELECTOR CIRCUIT
IMAGE MEMORY
308
LINE BUFFER
309
312
DISPLAY LINE SELECTOR CIRCUIT
DISPLAY SECTION
310

FIG. 31

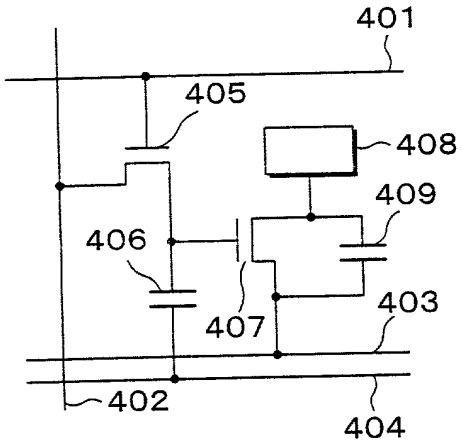
401
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FIG. 32

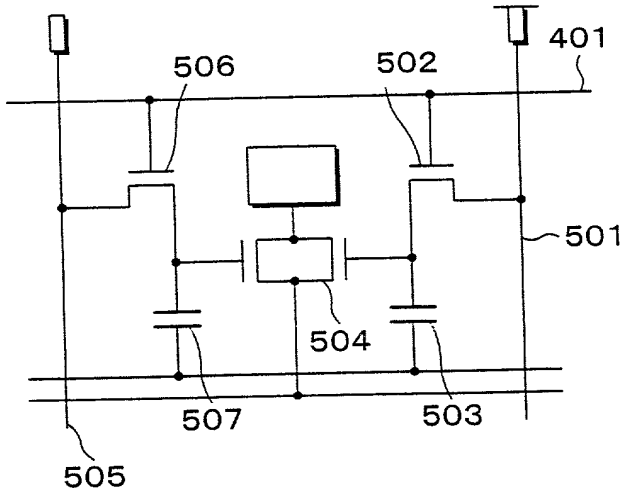
506
502
401
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FIG. 33

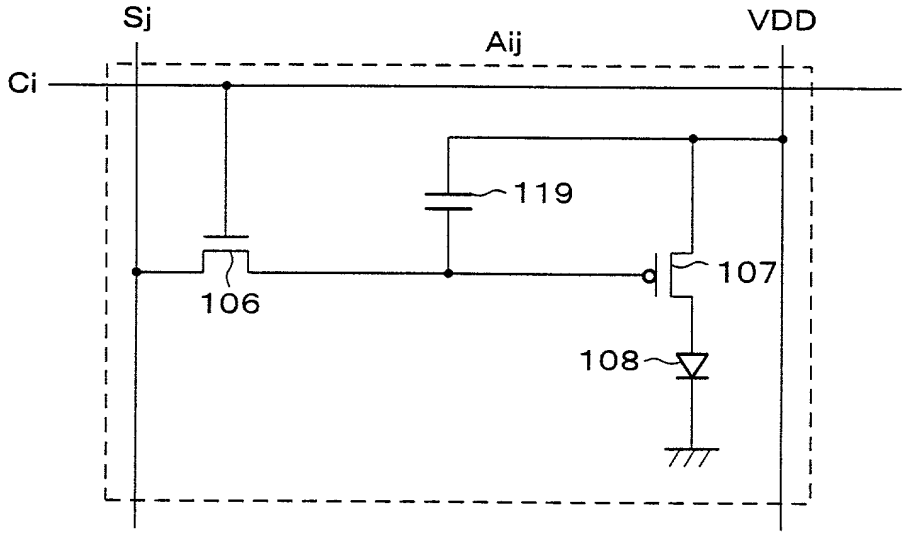

FIG. 34

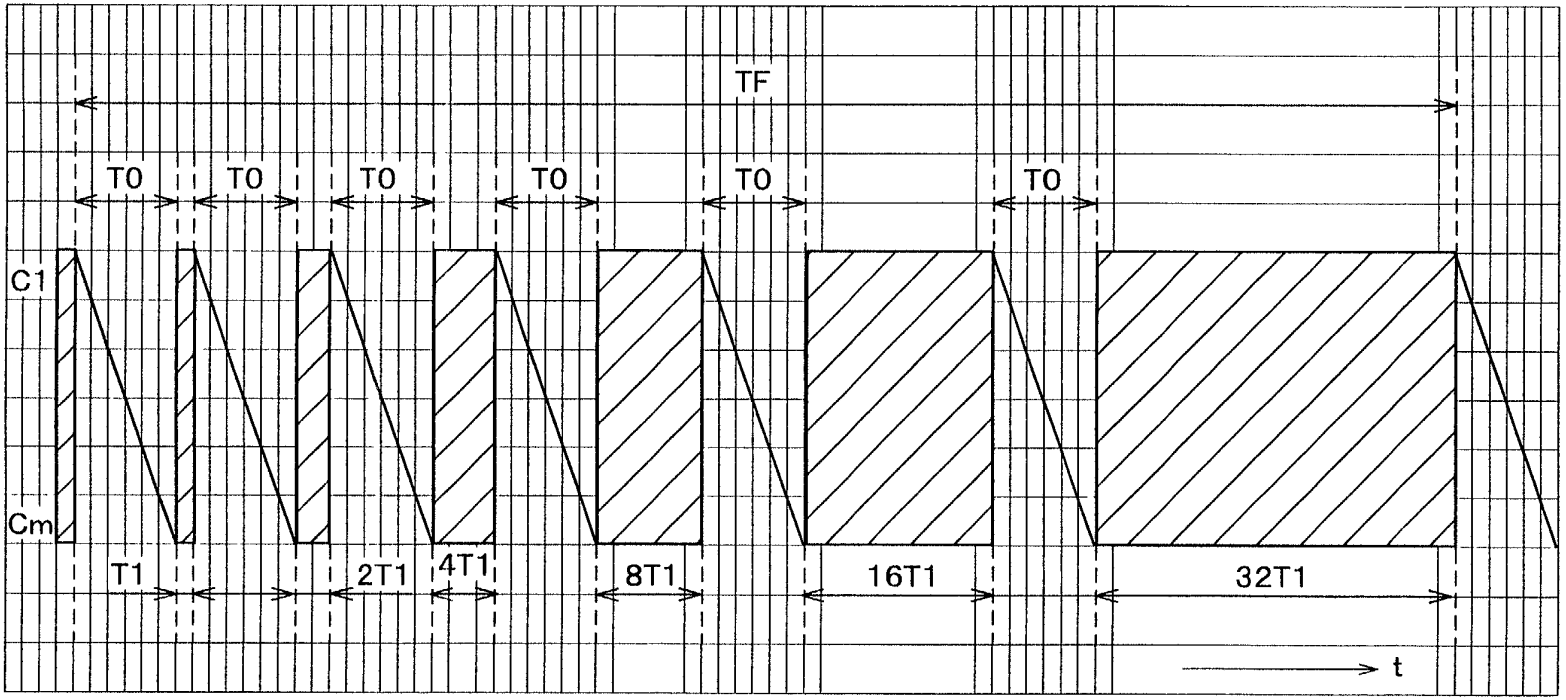

FIG. 35